Multilevel Operation and Input Power Balancing for a Dual Two-Level Inverter with Insulated DC Sources

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***Abstract*—A multilevel inverter topology feeding a three-phase open-end winding machine is analyzed in this paper. The scheme is based on the use of two insulated dc supplies, each one feeding a standard two-level three-phase inverter. The three-phase six-wire winding is connected across the output terminals of the two inverters. A new modulation technique that is able to regulate the sharing of the output power between the two dc sources in each switching cycle is presented. The performance of the whole system has been verified by both numerical and experimental tests.**

***Index Terms*—Dual two-level inverter, power sharing, space vector modulation, three-level inverter.**

I. Introduction

THE MULTILEVEL inverter technology has been widely recognized as a viable solution to overcome the voltage limits of power switching converters in the area of high-power medium-voltage drive systems. As it is known, multilevel converters are able to generate output voltage waveforms consisting in a large number of steps. In this way, high voltages can be synthesized using voltage sources with lower levels, with the additional benefit of a reduced harmonic distortion and lower dv/dt in the output voltages. These features have made multilevel converters suitable either for medium-voltage high-power motor drives or for low-voltage high-efficiency conversion systems.

Several multilevel inverter topologies have been introduced in the last ten years, the most important of them being the diode-clamped, the capacitor-clamped, and the cascaded converter [1].

Among the cascaded converters, the dual two-level inverter configuration has received large attention due to the simplicity of the power stage. It is based on two standard three-phase voltage source inverters supplied by two separate dc sources. The load is a three-phase machine in the open-end winding configuration [2]–[6], as shown in Fig. 1. The presence of two insulated dc supplies inherently eliminates common-mode currents and makes it possible to achieve the maximum output voltage without the need of a common-mode reactor [7]–[9]. Furthermore, the dual inverter topology has a high reliability because in case of fault in one inverter, its output terminals can be short-circuited, and the system can operate using the healthy inverter as a standard three-phase two-level inverter. In this way, the motor load can be supplied with the rated current (i.e., rated torque) up to half of the rated voltage (i.e., half of the rated speed).

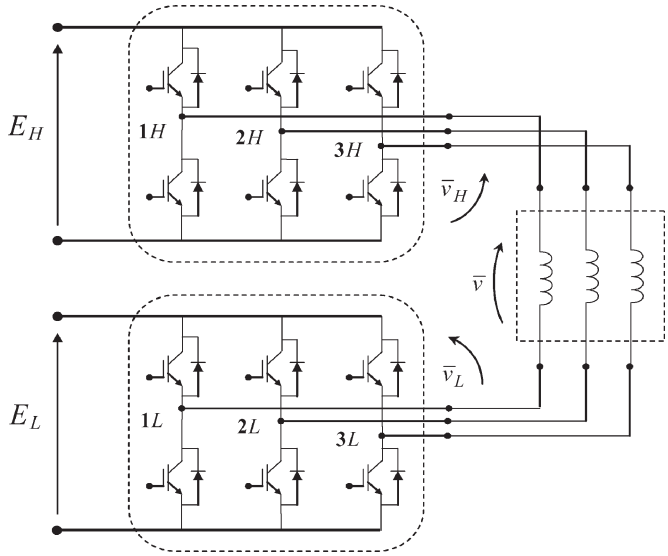

Fig. 1. Electrical scheme of the multilevel converter.

The proposed dual two-level inverter configuration can be usefully implemented when using a battery supply system because, in this case, it is very simple to split the dc supply into two electrically separated dc sources.

The dual two-level converter can also be considered as an alternative solution to either six-phase or dual three-phase drive systems, since it requires both the same number and the same sizing of switching components [10], [11].

Being the converter supplied by two distinct sources, in several applications, it is necessary to regulate the power flow from the two sources. This requirement can be demanded in order to equalize the state of charge of two banks of batteries or to exploit the different characteristics of two sources, e.g., generators and batteries. The power regulation capability of this converter was early described in [12] with reference to the averaged quantities. In [13], a simple commutation strategy based on six-step commutation, allowing power balancing, was

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also presented. Many other papers are related to the definition of a modulation strategy for generating multilevel voltage waveforms [14] or based on the application of a synchronized pulsewidth modulation (PWM) method [15].

In this paper, a new modulation technique is presented, which is able both to perform multilevel operation and to regulate the load power sharing between the two dc sources within each switching period [16], [17]. Furthermore, the problem of simultaneous leg commutations and its effect during the dead times is here addressed.

The discussion of the converter scheme shown in Fig. 1, the implementation of the multilevel modulation strategy, the definition of a suitable switching sequence, and the analysis of the power sharing constraints are presented in Sections II–V respectively. In Sections VI and VII, the behavior of the proposed control strategy for the dual two-level inverter is verified by a complete set of simulation results and experimental tests carried out on a full-scale prototype.

II. Principle of Operation

With reference to the scheme in Fig. 1 and using the space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter can be expressed as a function of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter H and inverter L, respectively, as follows:

$$\bar{v} = \bar{v}_H + \bar{v}_L. \tag{1}$$

Assuming $E_H = E_L = E$, the voltages $\bar{v}_H$ and $\bar{v}_L$ are given by

$$\begin{aligned} \bar{v}_H &= \frac{2}{3}E\left(S_{1H} + S_{2H}e^{j\frac{2}{3}\pi} + S_{3H}e^{j\frac{4}{3}\pi}\right) \\ \bar{v}_L &= -\frac{2}{3}E\left(S_{1L} + S_{2L}e^{j\frac{2}{3}\pi} + S_{3L}e^{j\frac{4}{3}\pi}\right) \end{aligned} \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverter legs.

The combination of the eight switch configurations of each inverter yields 64 possible switching states for the whole multilevel converter, corresponding to 18 different output active voltage vectors and one null vector, as represented by the red dots in Fig. 2. By using the space vector modulation (SVM) technique, these 19 voltage vectors can be modulated to obtain any output voltage vector lying inside the outer hexagon, having a side length of 4/3 E. In particular, with reference to sinusoidal steady-state operating conditions, the maximum magnitude of the output voltage vector $\bar{v}^*$, which can be generated by the converter, is $2/\sqrt{3}\ E$ (i.e., the radius of the inscribed circle).

The outer hexagon can be subdivided in 24 identical triangles which can be associated to three different types of regions. As shown in Fig. 2, there are 6 inner triangles (region ①—dashed), 6 intermediate triangles (region ②—white), and 12 outer triangles (region ③—dotted).

Within each switching period, the reference output voltage vector $\bar{v}^*$ can be synthesized as the sum of the voltage vectors $\bar{v}_H^*$, $\bar{v}_L^*$ generated by the two inverters, according to (1). Introducing the voltage ratio k and imposing the inverter voltage vectors $\bar{v}_H^*$, $\bar{v}_L^*$ to be in phase with the output voltage vector $\bar{v}^*$ yield

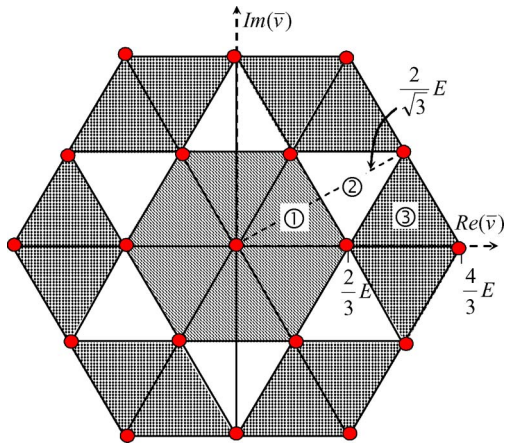


Fig. 2. Highlight of the triangles in three different regions ①, ②, and ③.

$$\begin{cases} \bar{v}_H^* = k\bar{v}^* \\ \bar{v}_L^* = (1-k)\bar{v}^*. \end{cases} \tag{3}$$

The condition for the inverter voltages to be in phase leads to the minimum value for $\bar{v}_H^*$, $\bar{v}_L^*$. Furthermore, having the two inverters the same current $(\bar{i})$, the coefficient k also defines the output power of the two inverters (p_H, p_L) as follows:

$$p = \frac{3}{2}\bar{v}^* \cdot \bar{i} = p_H + p_L \begin{cases} p_H = \frac{3}{2}\bar{v}_H^* \cdot \bar{i} = k \cdot p \\ p_L = \frac{3}{2}\bar{v}_L^* \cdot \bar{i} = (1-k) \cdot p. \end{cases} \tag{4}$$

The coefficient k, which determines the power sharing between the two inverters, has a limited variation range depending on the value of the reference output voltage $\bar{v}^*$. The possible values of k will be discussed in Section V.

III. Multilevel Operation

This section deals with the methods that can be utilized to generate the reference output voltage through the vector composition of the two inverter voltage vectors.

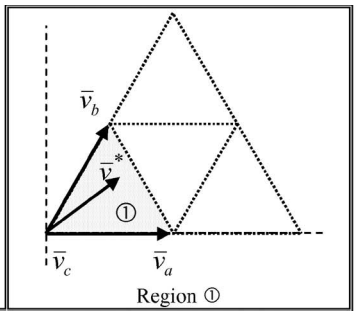
A correct multilevel operation requires the output voltage vector $\bar{v}^*$ to be synthesized by modulating three voltage vectors, corresponding to the vertices of the triangle in which the output voltage vector $\bar{v}^*$ lies. Taking into account the regions defined in Fig. 2, $\bar{v}^*$ can be synthesized in each switching period using the main output vectors $\bar{v}_a$, $\bar{v}_b$, $\bar{v}_c$, as shown in Fig. 3.

The output voltage $\bar{v}^*$ can be expressed by means of the duty cycles a, b, c of the three adjacent main vectors as follows:

$$\bar{v}^* = a\bar{v}_a + b\bar{v}_b + c\bar{v}_c \tag{5}$$

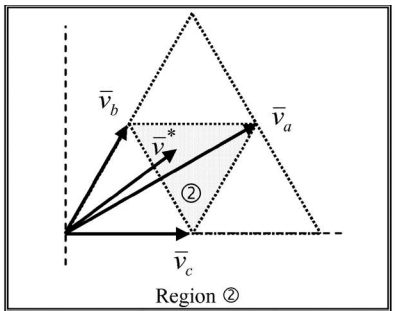
where the duty cycles a, b, c are given by

$$\begin{cases} a = \frac{(\bar{v}^* - \bar{v}_c)\cdot j(\bar{v}_b - \bar{v}_c)}{(\bar{v}_a - \bar{v}_c)\cdot j(\bar{v}_b - \bar{v}_c)} \\ b = -\frac{(\bar{v}^* - \bar{v}_c)\cdot j(\bar{v}_a - \bar{v}_c)}{(\bar{v}_a - \bar{v}_c)\cdot j(\bar{v}_b - \bar{v}_c)} \\ c = 1 - (a+b) = 1 - \frac{(\bar{v}^* - \bar{v}_c)\cdot j(\bar{v}_b - \bar{v}_a)}{(\bar{v}_a - \bar{v}_c)\cdot j(\bar{v}_b - \bar{v}_c)}. \end{cases} \tag{6}$$



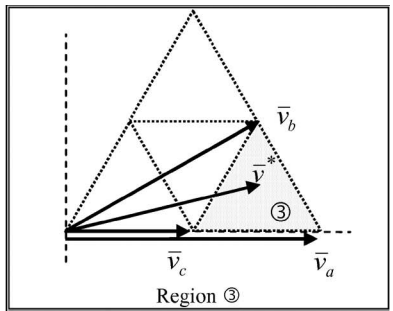
Region ①

main duty-cycle	a		b		c
$\bar{v} = \bar{v}_H + \bar{v}_L$	$\bar{v}_a = \bar{v}_\alpha$		$\bar{v}_b = \bar{v}_\beta$		$\bar{v}_c = \bar{0}$
$\bar{v}_H$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\beta$	$\bar{0}$	$\bar{0}$
$\bar{v}_L$	$\bar{0}$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\beta$	$\bar{0}$
sub duty-cycle	a'	a''	b'	b''	c



Region ②

a		b		c	
$\bar{v}_a = \bar{v}_\alpha + \bar{v}_\beta$		$\bar{v}_b = \bar{v}_\beta$		$\bar{v}_c = \bar{v}_\alpha$	
$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{0}$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$
$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{0}$	$\bar{0}$	$\bar{v}_\alpha$
a'	a''	b'	b''	c'	c''



Region ③

a	b		c	
$\bar{v}_a = 2\bar{v}_\alpha$	$\bar{v}_b = \bar{v}_\alpha + \bar{v}_\beta$		$\bar{v}_c = \bar{v}_\alpha$	
$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\alpha$
$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$
a	b'	b''	c'	c''

Fig. 3. Vector composition to obtain the reference output voltage vector in regions ①, ②, and ③.

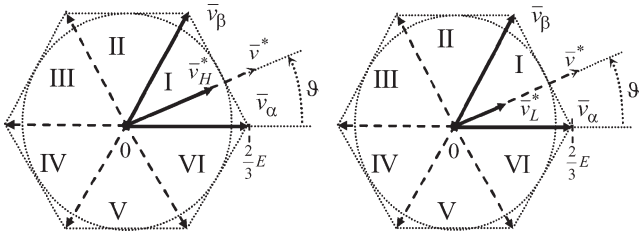


Fig. 4. Reference voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha$, $\bar{v}_\beta$.

According to the choice expressed by (3), the inverter voltage vectors $\bar{v}_H^*$ and $\bar{v}_L^*$ are in phase and lie in the same sector, as shown in Fig. 4. As a consequence, the two inverters synthesize $\bar{v}_H^*$ and $\bar{v}_L^*$ by modulating the same adjacent active vectors $\bar{v}_\alpha$, $\bar{v}_\beta$. The resulting output voltage vectors of the two inverters are

$$\begin{cases} \bar{v}_H^* = \alpha_H \bar{v}_\alpha + \beta_H \bar{v}_\beta + \gamma_H \bar{0} \\ \bar{v}_L^* = \alpha_L \bar{v}_\alpha + \beta_L \bar{v}_\beta + \gamma_L \bar{0}. \end{cases} \tag{7}$$

In (7), α_H, β_H, and γ_H are the duty cycles of active vectors $\bar{v}_\alpha$, $\bar{v}_\beta$ and null vector, respectively, for the inverter H. In the same way, α_L, β_L, and γ_L are the duty cycles of active vectors $\bar{v}_\alpha$, $\bar{v}_\beta$ and null vector, respectively, for the inverter L.

By using standard SVM equations, the duty cycles of inverters H and L can be calculated by the following equations:

$$\begin{cases} \alpha_H = \frac{\bar{v}_H^* \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \beta_H = -\frac{\bar{v}_H^* \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta}, \quad \gamma_H = 1 - (\alpha_H + \beta_H) \end{cases} \tag{8}$$

$$\begin{cases} \alpha_L = \frac{\bar{v}_L^* \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \beta_L = -\frac{\bar{v}_L^* \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta}, \quad \gamma_L = 1 - (\alpha_L + \beta_L). \end{cases} \tag{9}$$

In order to achieve a correct multilevel operation, it is required to apply to the load, instant by instant, one of the three main output voltage vectors $(\bar{v}_a, \bar{v}_b, \bar{v}_c)$ adjacent to the reference output voltage vector $\bar{v}^*$. For this purpose, the active vectors $(\bar{v}_\alpha, \bar{v}_\beta)$ and null vectors of the two inverters must be properly combined.

With reference to regions ①, ②, and ③ shown in Fig. 3, three different vector combinations can be defined, according to the following equations:

Region ①	Region ②	Region ③
$\begin{cases} \bar{v}_a = \bar{v}_\alpha + 0 \\ \bar{v}_b = \bar{v}_\beta + 0 \\ \bar{v}_c = 0 + 0 \end{cases}$	$\begin{cases} \bar{v}_a = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_b = \bar{v}_\beta + 0 \\ \bar{v}_c = \bar{v}_\alpha + 0 \end{cases}$	$\begin{cases} \bar{v}_a = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_b = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_c = \bar{v}_\alpha + 0. \end{cases}$

(10)

As the two inverters H and L always modulate with the same active vectors $\bar{v}_\alpha$, $\bar{v}_\beta$ in each switching period, each main output voltage vector can be generated by two different combinations of inverter voltage vectors $\bar{v}_\alpha$, $\bar{v}_\beta$, 0. These combinations are represented in the table included in Fig. 3 for regions ①, ②, and ③.

As an example, when $\bar{v}^*$ is in region ①, the main output voltage vector $\bar{v}_a$ can be applied subdividing its main duty cycle a in two sub duty cycles a', a'', so that $a = a' + a''$. In a', inverter H generates $\bar{v}_\alpha$ and inverter L generates 0, whereas in a'', inverter L generates $\bar{v}_\alpha$ and inverter H generates 0. Similar criteria are adopted for generating the main voltage vectors $\bar{v}_a$, $\bar{v}_b$, $\bar{v}_c$ in the different regions.

By using the vector combinations given in (10) and the sub duty cycles a', a'', b', b'', c', c'' defined in Fig. 3, it is possible to group the sub duty cycles in order to highlight the duty cycles of the two inverters $(\alpha_H, \beta_H, \gamma_H, \alpha_L, \beta_L, \gamma_L)$, as shown in Table I.

The values of the sub duty cycles can be determined for the three regions on the basis of the main duty cycles and the duty cycles of the two inverters as follows:

Region ①	Region ②	Region ③
$\begin{cases} a' = \alpha_H \\ a'' = \alpha_L \\ b' = \beta_H \\ b'' = \beta_L \\ c \; is \; known \\ - \end{cases}$	$\begin{cases} a' + c' = \alpha_H \\ a'' + b'' = \beta_H \\ b' + c'' = \gamma_H \\ a'' + c'' = \alpha_L \\ a' + b' = \beta_L \\ b'' + c' = \gamma_L \end{cases}$	$\begin{cases} a \; is \; known \\ - \\ b' = \beta_H \\ b'' = \beta_L \\ c' = \gamma_H \\ c'' = \gamma_L. \end{cases}$

(11)

TABLE I
SUB-DUTY-CYCLE DETERMINATION FOR INVERTERS H AND L

	Region ①					Region ②						Region ③				
main voltages	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$
sub duty-cycle	a'	b'	c	b''	a''	c'	a'	b'	c''	a''	b''	c'	b'	a	b''	c''

$\bar{v}_H$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{0}$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\beta$	$\bar{0}$	$\bar{v}_\beta$	$\bar{v}_\alpha$
duty-cycle	α_H	β_H	γ_H	α_H	γ_H	β_H	γ_H	β_H	α_H

$\bar{v}_L$	$\bar{0}$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{0}$
duty-cycle	γ_L	β_L	α_L	γ_L	β_L	α_L	γ_L	α_L	β_L	γ_L

It can be noted that for regions ① and ③, the sub duty cycles are five, whereas for region ②, the sub duty cycles are six and can be determined by solving a system of six equations. Only five of these equations are linearly independent. Then, the system of equations (11) for region ② can be solved in parametric form, assuming c' as parameter.

Introducing the condition that all sub duty cycles must be greater than zero $(a', a'', b', b'', c', c'' \geq 0)$, the admissible variation range of parameter c' is given by the most restrictive among the following equations:

$$\begin{cases} c' \geq 0 \\ c' \geq \gamma_L - \beta_H \\ c' \geq \alpha_H - \beta_L \end{cases} \quad \text{and} \quad \begin{cases} c' \leq \alpha_H \\ c' \leq \gamma_L \\ c' \leq \alpha_L + \gamma_L - \beta_H. \end{cases} \tag{12}$$

By choosing a value for c' inside this range, the values of the other sub duty cycles in region ② are determined as follows:

$$\begin{cases} a' = \alpha_H - c' \\ a'' = \beta_H - \gamma_L + c' \\ b' = \beta_H - \alpha_H + c' \\ b'' = \gamma_L - c' \\ c'' = \alpha_L - \beta_L + \gamma_L - c'. \end{cases} \tag{13}$$

Once the sub duty cycles have been determined in each switching period, they should be properly distributed in a switching sequence in order to implement a traditional symmetric modulation for both inverters.

IV. DETERMINATION OF THE SWITCHING SEQUENCE

The minimization of the number of switch commutations and the application of correct voltage vectors during commutations are the two basic criteria used in this section to define the switching sequence.

As it is known, when a leg commutation occurs [branch switch over (BSO)], a dead time is introduced in the firing signals for the switches' safety. Dead times lead to an output voltage level depending only on the direction of the output current. In particular, during dead times, the state of the commutating leg is "0" for source current and "1" for sink current.

When the commutation between two voltage vectors is performed by one BSO only, the dual two-level inverter applies the outgoing or the incoming voltage vectors depending on the sign of the output current in the commutating leg. Thus, the voltage vector applied to the load during the dead time is one of the three expected adjacent main vectors $\bar{v}_a$, $\bar{v}_b$, $\bar{v}_c$. On the contrary, when the commutation between two voltage vectors is obtained by two simultaneous BSOs, the voltage vector could be different from $\bar{v}_a$, $\bar{v}_b$, $\bar{v}_c$ during the dead time, leading to a spurious voltage pulse.

TABLE II
SWITCHING SEQUENCE IN REGION ①

$\bar{v}$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$	$\bar{v}_a$
sub d.cycle	$\frac{b''}{2}$	$\frac{c}{4}$	$\frac{a'}{2}$	$\frac{b'}{2}$	$\frac{c}{4}$	$\frac{b''}{2}$	$\frac{a''}{2}$	$\frac{c}{4}$	$\frac{b'}{2}$	$\frac{a'}{2}$	$\frac{c}{4}$	$\frac{a''}{2}$
$\bar{v}_H$	$\bar{0}$		$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{0}$				$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{0}$	
s_{H1}	0	0	1	1	1	1	1	1	1	1	0	0
s_{H2}	0	0	0	1	1	1	1	1	1	0	0	0
s_{H3}	0	0	0	0	1	1	1	1	0	0	0	0
s_{L1}	0	0	0	0	0	0	0	1	1	1	1	0
s_{L2}	0	0	0	0	0	0	1	1	1	1	1	1
s_{L3}	1	0	0	0	0	1	1	1	1	1	1	1
$\bar{v}_L$	$\bar{v}_\beta$		$\bar{0}$			$\bar{v}_\beta$	$\bar{v}_\alpha$		$\bar{0}$			$\bar{v}_\alpha$

The proposed switching sequences for regions ①, ②, and ③ have been implemented by introducing a single turn-on and a single turn-off in a switching period for each one of the six legs, as in traditional continuous PWM.

The analysis carried out on possible switching sequences has shown that for regions ① and ③, it is possible to implement a switching sequence having a single BSO for each commutation step, as shown in Tables II and III, respectively. In particular, the proposed 12 step sequences are obtained by halving the sub duty cycles and generating voltage vectors with symmetry within the switching period for each one of the two inverters. Unfortunately, a switching sequence having a single BSO for each commutation step has not been found for region ②. The better switching sequence developed for region ② is shown in Table IV. The two dashed squares underline commutation steps involving two simultaneous BSOs. In these cases, the voltage vector applied to the load during the dead time depends on the direction of the output current in the two commutating legs, leading to four possible output voltage vectors.

The four cases have been studied for both the commutation steps, and the corresponding output voltage vectors are given in Table V, as a function of the sign of the load currents. It can

TABLE III
SWITCHING SEQUENCE IN REGION ③

$\bar{v}$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$	$\bar{v}_a$
sub d.cycle	$\frac{c'}{2}$	$\frac{a}{4}$	$\frac{b''}{2}$	$\frac{c''}{2}$	$\frac{b''}{2}$	$\frac{a}{4}$	$\frac{b'}{2}$	$\frac{c'}{2}$	$\frac{b'}{2}$	$\frac{a}{4}$	$\frac{c''}{2}$	$\frac{a}{4}$
$\bar{v}_H$	$\bar{0}$	$\bar{v}_\alpha$					$\bar{v}_\beta$	$\bar{0}$	$\bar{v}_\beta$	$\bar{v}_\alpha$		
s_{H1}	0	1	1	1	1	1	1	1	1	1	1	1
s_{H2}	0	0	0	0	0	0	1	1	1	0	0	0
s_{H3}	0	0	0	0	0	0	0	1	0	0	0	0
s_{L1}	0	0	0	0	0	0	0	0	0	0	1	0
s_{L2}	1	1	0	0	0	1	1	1	1	1	1	1
s_{L3}	1	1	1	0	1	1	1	1	1	1	1	1
$\bar{v}_L$	$\bar{v}_\alpha$		$\bar{v}_\beta$	$\bar{0}$	$\bar{v}_\beta$		$\bar{v}_\alpha$				$\bar{0}$	$\bar{v}_\alpha$

TABLE IV
SWITCHING SEQUENCE IN REGION ②

$\bar{v}$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_c$	$\bar{v}_a$	$\bar{v}_b$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$	$\bar{v}_b$	$\bar{v}_a$	$\bar{v}_c$
sub d.cycle	$\frac{c'}{2}$	$\frac{a'}{2}$	$\frac{b'}{2}$	$\frac{c''}{2}$	$\frac{a''}{2}$	$\frac{b''}{2}$	$\frac{b''}{2}$	$\frac{a''}{2}$	$\frac{c''}{2}$	$\frac{b'}{2}$	$\frac{a'}{2}$	$\frac{c'}{2}$
$\bar{v}_H$	$\bar{v}_\alpha$		$\bar{0}$		$\bar{v}_\beta$				$\bar{0}$		$\bar{v}_\alpha$	
s_{H1}	1	1	0	0	1	1	1	1	1	1	1	1
s_{H2}	0	0	0	0	1	1	1	1	1	1	0	0
s_{H3}	0	0	0	0	0	0	0	0	1	1	0	0
s_{L1}	0	0	0	0	0	1	1	0	0	0	0	0
s_{L2}	0	0	0	1	1	1	1	1	1	0	0	0
s_{L3}	0	1	1	1	1	1	1	1	1	1	1	0
$\bar{v}_L$	$\bar{0}$	$\bar{v}_\beta$		$\bar{v}_\alpha$		$\bar{0}$		$\bar{v}_\alpha$		$\bar{v}_\beta$		$\bar{0}$

TABLE V
OUTPUT VOLTAGE VECTORS APPLIED DURING DEAD TIMES IN REGION ②

i_1	>0	>0	<0	<0	x	x	x	x
i_2	>0	<0	>0	<0	>0	>0	<0	<0
i_3	x	x	x	x	>0	<0	>0	<0
s_{H1}	0	0	1	1	1	1	1	1
s_{H2}	0	1	0	1	0	0	1	1
s_{H3}	0	0	0	0	0	1	0	1
$\bar{v}_H$	$\bar{0}$	$\frac{2}{3}Ee^{j\frac{2}{3}\pi}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{-j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\bar{0}$
$\bar{v}_L$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$
$\bar{v}$	$\frac{2}{3}Ee^{j0}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$	$\frac{4}{3}Ee^{j0}$	$\frac{2}{\sqrt{3}}Ee^{j\frac{\pi}{6}}$	$\frac{2}{\sqrt{3}}Ee^{j\frac{\pi}{6}}$	$\frac{2}{3}Ee^{j0}$	$\frac{4}{3}Ee^{j\frac{\pi}{3}}$	$\frac{2}{3}Ee^{j\frac{\pi}{3}}$
	$\bar{v}_c$	$\bar{v}_b$	$2\bar{v}_c$	$\bar{v}_a$	$\bar{v}_a$	$\bar{v}_c$	$2\bar{v}_b$	$\bar{v}_b$
	OK	OK	OUT	OK	OK	OK	OUT	OK

be noted that there are only two operating conditions yielding to the application of an output voltage different from $\bar{v}_a$, $\bar{v}_b$, $\bar{v}_c$, which are $\{i_1 < 0,\ i_2 > 0\}$ and $\{i_2 < 0,\ i_3 > 0\}$. These conditions are graphically represented in the vector diagram of Fig. 5 by two shaded areas. The same diagram shows that for load current phase angle (φ) ranging from -30° to $+30^\circ$, the

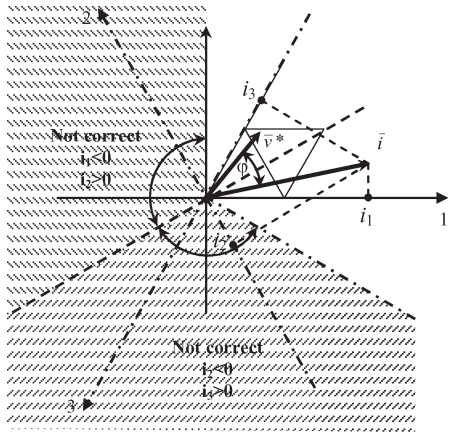


Fig. 5. Load current effects during dead times.

two previous conditions do not occur, and the voltage vector applied during the dead time always corresponds to one of the vertices of region ② $(\bar{v}_a, \bar{v}_b, \bar{v}_c)$. It is worth noting that even if φ is greater than $+30^\circ$ or lower than -30°, the multilevel operation is anyhow obtained, except for the possible presence of voltage pulse during dead times.

V. REGULATION OF THE POWER SHARING AND MODULATION LIMITS

The constraints of duty cycles introduced in (8) and (9) can be expressed as

$$\begin{cases} \alpha_H \geq 0 \\ \beta_H \geq 0 \\ \alpha_H + \beta_H \leq 1 \end{cases} \qquad \begin{cases} \alpha_L \geq 0 \\ \beta_L \geq 0 \\ \alpha_L + \beta_L \leq 1. \end{cases} \tag{14}$$

These constraints introduce a limit in the range of variation of the power sharing coefficient k. In particular, the range of variation of k can be expressed as a function of the desired output vector $\bar{v}^*$. Introducing (8) and (9) in (14) and taking (3) into account lead to

$$\begin{cases} \frac{k\bar{v}^* \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\frac{k\bar{v}^* \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \frac{k\bar{v}^* \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1 \end{cases} \qquad \begin{cases} \frac{(1-k)\bar{v}^* \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\frac{(1-k)\bar{v}^* \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \frac{(1-k)\bar{v}^* \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1. \end{cases} \tag{15}$$

Assuming sinusoidal output voltages ($\bar{v}^* = V^* e^{j\vartheta}$) and introducing the modulation index $m = V^*/(2/\sqrt{3})E$, being $0 \leq m \leq 1$ the range for linear modulation, the solution of (15) is

$$\frac{1}{2} - a \leq k \leq \frac{1}{2} + a \tag{16}$$

where

$$a = \frac{1-m}{2m}. \tag{17}$$

By means of (16) and (17), the possible values of k can be determined as a function of the modulation index m. This relationship is graphically shown in Fig. 6. The dashed area defines the possible values of k and then determines to which extent the power sharing between the two inverters can be

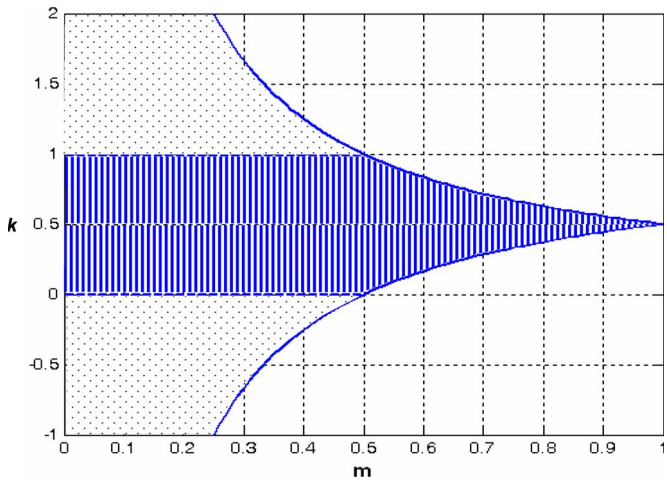


Fig. 6. Limits of the power sharing coefficient k versus the modulation index m.

TABLE VI
MAIN SIMULATION PARAMETERS FOR THE DUAL INVERTER SYSTEM

dc bus voltages	$E_H = E_L = 100$ V
output frequency	$f_o = 50$ Hz
six wires load	passive, series RL
load resistance	$R = 10\ \Omega$
load inductance	$L = 10$ mH
switching frequency	$f_s = 2$ kHz

changed. By analyzing Fig. 6, the following considerations can be made.

1) If the maximum output voltage is required (i.e., $m = 1$), it is not possible to regulate the power sharing between the two dc sources. In this case, only the value $k = 0.5$ is acceptable, and the two sources generate the same voltages and supply the same power to the load.
2) For $0.5 \leq m \leq 1$, the coefficient k is limited as a function of m, showing a decreasing range of variation as m increases.
3) For $m < 0.5$, the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if k is set to 0, all the load power is supplied by inverter L, whereas if k is set to 1, all the load power is supplied by inverter H. This is a very important feature of this converter since it is possible to supply the load by using one inverter only, if necessary.
4) For $m < 0.5$, the power sharing coefficient k could be greater than unity or lower than zero. This means that an amount of power can be transferred from one dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase opposition, as shown by (3). This feature is interesting when using batteries, because it is possible to balance the charge status by transferring energy from one battery to the other.

VI. SIMULATION RESULTS

The dual two-level converter has been implemented in the Simulink environment of Matlab by using appropriate S functions. The system parameters are given in Table VI, and the

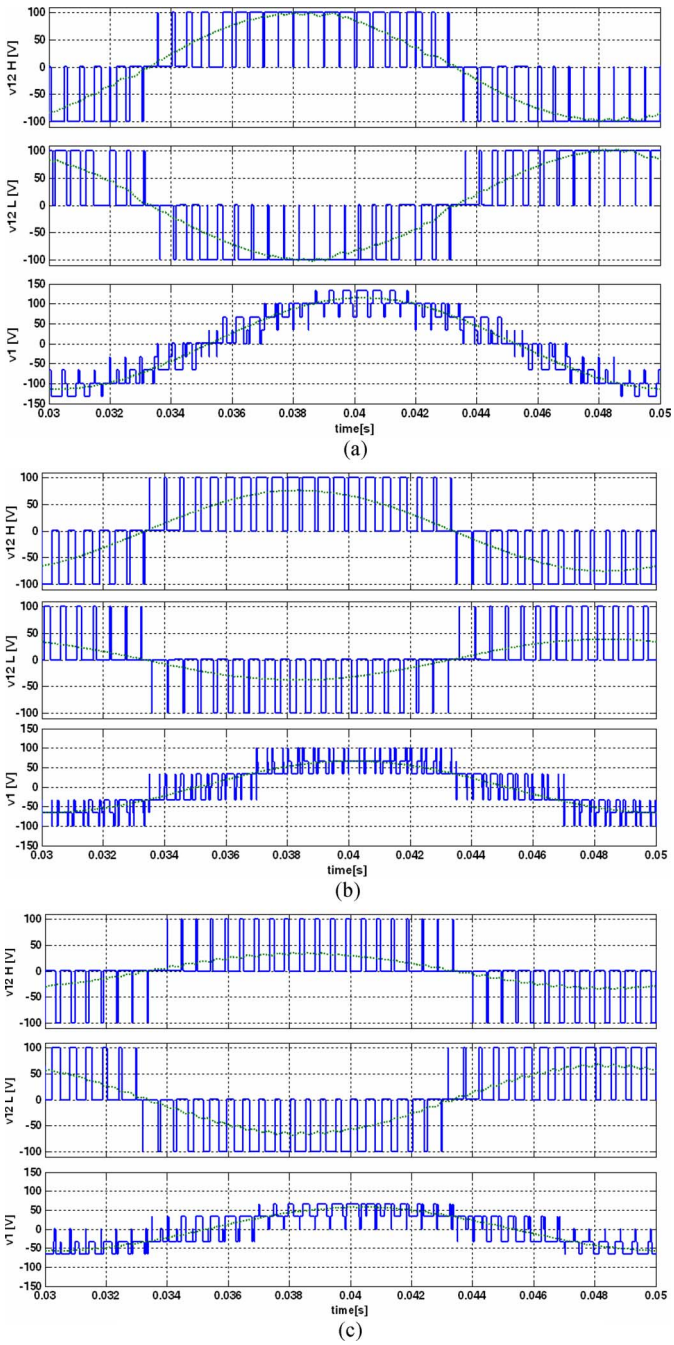


Fig. 7. Voltage waveforms for different values of m and k. From top to bottom: Line-to-line voltage generated by inverter H, line-to-line voltage generated by inverter L, and load phase voltage. (a) $m = 1$ ($v = 2/\sqrt{3}\ E$), $k = 1/2$ ($1 - k = 1/2$). (b) $m = 1/\sqrt{3}$ ($v = 2/3\ E$), $k = 2/3$ ($1 - k = 1/3$). (c) $m = 1/2$ ($v = 1/\sqrt{3}\ E$), $k = 1/3$ ($1 - k = 2/3$).

corresponding simulation results, based on the switching sequence shown in Tables II–IV, are shown in Fig. 7. In particular, both the instantaneous values (blue lines) and the averaged values within each cycle period (green lines) are represented.

Fig. 7(a) shows, from the top to the bottom, the line-to-line voltage of inverters H and L, and the load phase voltage with the maximum value of the modulation index $m = 1$ (i.e., $v = 2/\sqrt{3}\ E$), and $k = 1/2$. In this case, the two inverters generate the same voltages, supplying the same power to the load. It can be noted that the phase voltage is distributed on nine

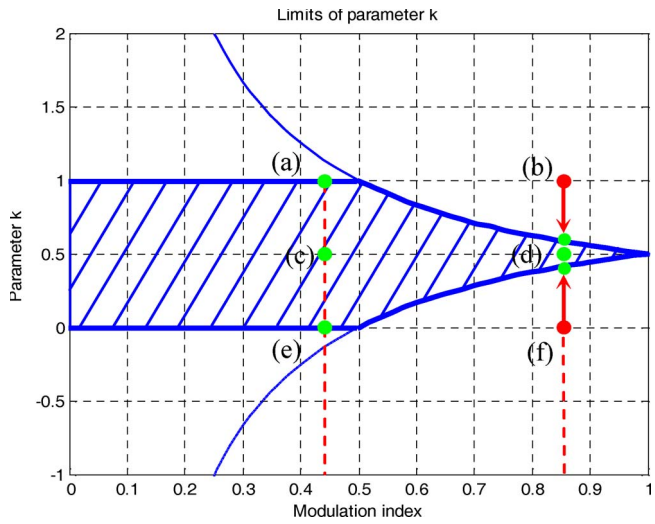


Fig. 8. Operating points considered for the tests of Fig. 9 on the diagram power sharing coefficient k versus modulation index m.

levels, meaning triangles of regions ② and ③ are involved in commutation.

Fig. 7(b) shows the same voltage waveforms as in Fig. 7(a) with $m = 1/\sqrt{3}$ (i.e., $v = 2/3\ E$), and $k = 2/3$. This value of m corresponds to the maximum output voltage vector that can be generated inside inner and intermediate triangles. In this case, the outer triangles (region ③) are not involved, and the phase voltage is distributed on the lower seven levels only. Being $k = 2/3$, the voltage generated by inverter H is twice the voltage generated by inverter L.

Fig. 7(c) shows the same waveforms as in Fig. 7(a) with $m = 1/2$ (i.e., $v = 1/\sqrt{3}\ E$), and $k = 1/3$. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the phase voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being $k = 1/3$, the voltage generated by inverter H is half the voltage generated by inverter L.

The correct multilevel modulation is proved by observing that in all cases shown in Fig. 7 for each switching period, the load phase voltage is distributed on three levels. These levels correspond to the voltage vectors $(\bar{v}_a, \bar{v}_b, \bar{v}_c)$ in the vertices of the triangle where the synthesized vector is located.

In order to validate the modulation limits and the power sharing capability presented in Section V, the working points (a), (b), (c), (d), (e), and (f) shown in Fig. 8 are investigated. The corresponding powers supplied from each inverter, p_H and p_L, are shown in Fig. 9, from (a) to (f). These figures are obtained by filtering the instantaneous powers with a second-order low-pass filter with a cutoff frequency of 100 Hz.

In Fig. 9(a), (c), and (e), (left column) the modulation index m is set to $\sqrt{3}/4$ ($\cong$ 0.433), and the desired power sharing parameter k is set to 1, 0.5, and 0, respectively. As expected, the inverter powers p_H and p_L follow the simple rule expressed by (4).

In Fig. 9(b), (d), and (f), (right column) the modulation index m is set to $\sqrt{3}/2$ ($\cong$ 0.866), and the desired power sharing parameter k is set to 1, 0.5, and 0, respectively.

With reference to the point (d) which is inside the operating region, the inverter is able to correctly operate in this condition.

With reference to points (b) and (f), which are outside of the operating region, the resulting working points are set at the intersection of $m = 0.866$ with the limit curves, as shown in Fig. (8). By applying (16), the actual power sharing parameters are $1/\sqrt{3}$ ($\cong$ 0.577) and $1 - 1/\sqrt{3}$ ($\cong$ 0.423), respectively. The power fluctuations shown in Fig. 9(b) and (f) are due to the voltage limits for each individual inverter. In fact, these limits are represented by a hexagon instead of a circle, as shown in Fig. 4, leading to six fluctuations for any fundamental period (i.e., 300 Hz in the present case of a fundamental frequency of 50 Hz). In order to remove these fluctuations, the control algorithm could be easily modified by limiting the individual inverter voltage within the inner circle of the hexagon.

VII. Experimental Results

The multilevel converter has been tested by using the prototype shown in Fig. 10. The main data of the power stage are reported in Table VII.

The control algorithm is based on the switching sequence presented in Tables II–IV. The proposed space vector modulation has been implemented on a control board based on TMS320F2812 DSP, operating with a clock frequency of 150 MHz, and using both the two independent three-phase PWM generators having a carrier frequency of 10 kHz. Despite of the complexity of implementation, no additional control hardware (e.g., FPGA) is used besides the DSP for the control of the switch commutations.

In order to verify the power balancing capability of the multilevel converter, the averaged line-to-line output voltages obtained with different values of k are investigated.

Fig. 11(a) shows the results obtained with $m = 1/2$ and $k = 1/2$. In this case, the line-to-line voltages generated by the two inverters have the same amplitude and are in phase opposition. The power delivered by the two inverters is the same.

Fig. 11(b) shows the results obtained with $m = 1/2$ and $k = 3/4$. In this case, the line-to-line voltages generated by the two inverters are unbalanced. Moreover, the power delivered to the load is unbalanced as the voltages.

Figs. 12 and 13 show the load phase voltage and current waveforms with reference to different values of the modulation index m.

Fig. 12 shows the phase voltage (upper trace) and the phase current (lower trace) with $m = 0.4$. In this condition, the output phase voltage is distributed on the lower five levels, since only the triangles corresponding to region ① are involved.

Fig. 13 shows the phase voltage (upper trace) and the phase current (lower trace) with $m = 0.8$. The output phase voltage is distributed on nine levels, since also the triangles in regions ② and ③ are involved for the modulation of the output voltages.

The experimental voltage and current waveforms show the effectiveness of the proposed control strategy both in terms of correct multilevel modulation and in terms of powersharing capability of the two inverters.

VIII. Conclusion

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding a three-phase

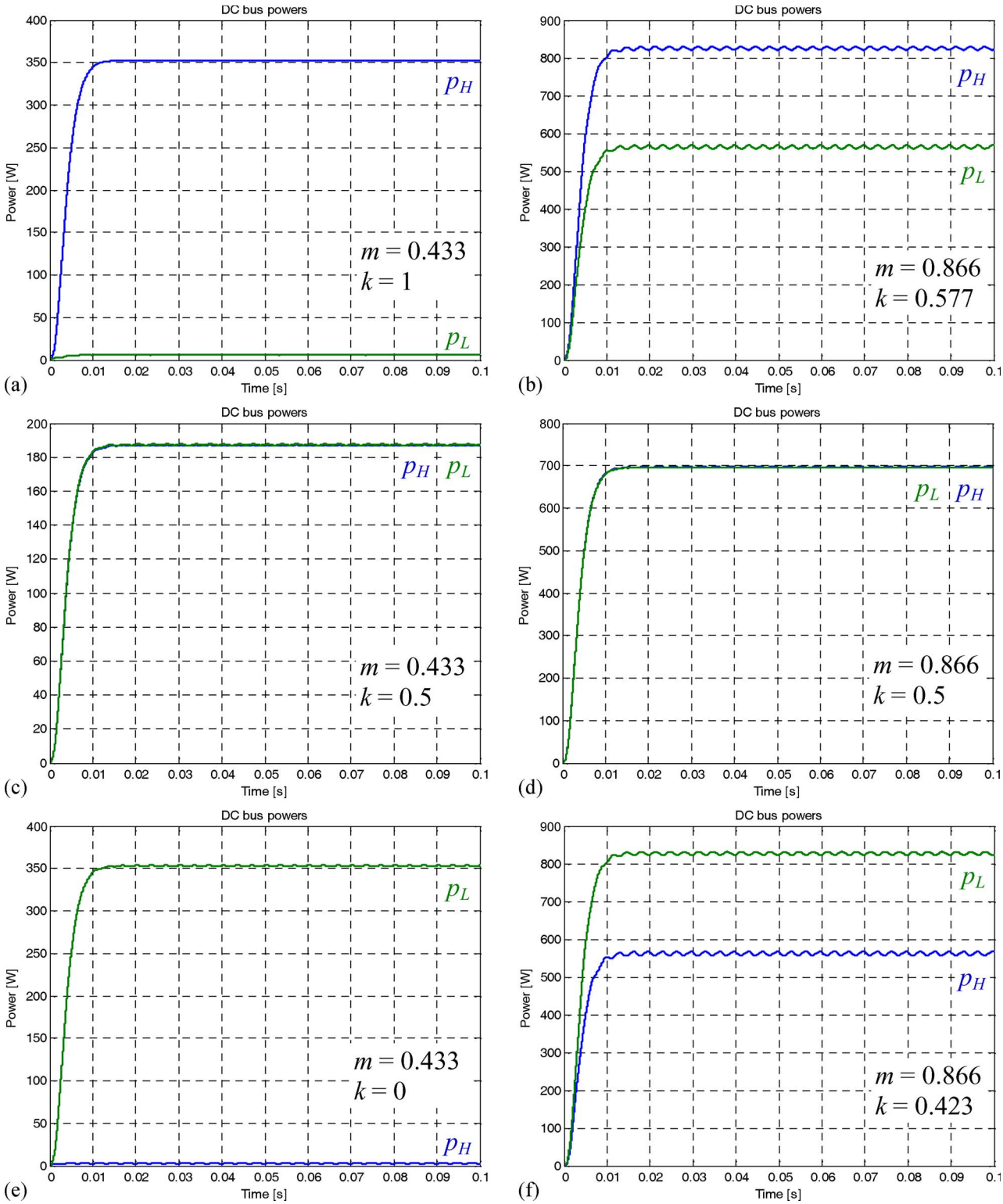


Fig. 9. Behavior of instantaneous powers (low-frequency component only) for operating points shown in Fig. 8.

machine with open-end windings has been analyzed in this paper. The dc supply insulation allows full dc bus utilization and avoids common-mode currents without the need of a common-mode reactor. This paper has been focused on the development of a modulation strategy that is able to regulate the power sharing between the dc sources and on the determination of a correct switching sequence for the two inverters. It has been shown that an unbalanced power sharing between the two inverters is possible and that the limits of the degree of unbalance can be determined as a function of the modulation index.

A switching sequence has been proposed, which ensures the correct multilevel operation and the possibility to limit the number of BSOs to one, except in the case of voltage vectors

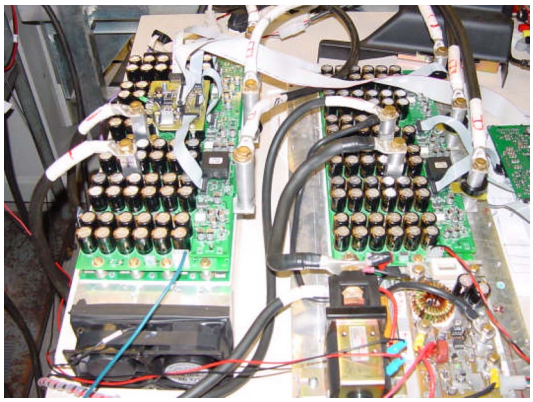


Fig. 10. Photograph of the power stage of the full-scale multilevel converter.

TABLE VII
CHARACTERISTICS OF THE POWER INVERTERS

supply system	lead acid battery 80V, 500Ah
rated dc voltage	$E = V_{dc} = 80$ V
rated output current	$I_{S(RMS)} = 180$ A
maximum output current (t = 60", t = 240")	$I_{SM1(RMS)} = 600$ A , $I_{SM2(RMS)} = 450$ A
technology	MOSFETs - parallel connected on an Insulated Metal Substrate (IMS)

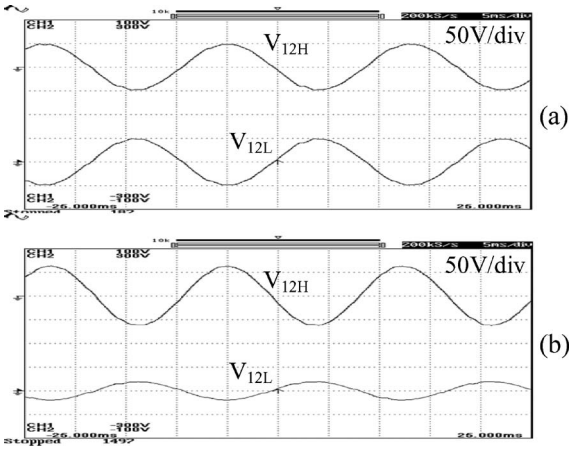


Fig. 11. Averaged line-to-line output voltages: (a) $m = 1/2$, $k = 1/2$ (balanced); (b) $m = 1/2$, $k = 3/4$ (unbalanced).

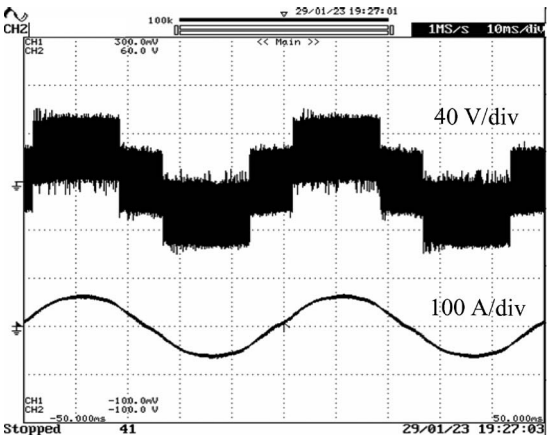


Fig. 12. Phase voltage (over five levels) and current waveforms with $m = 0.4$.

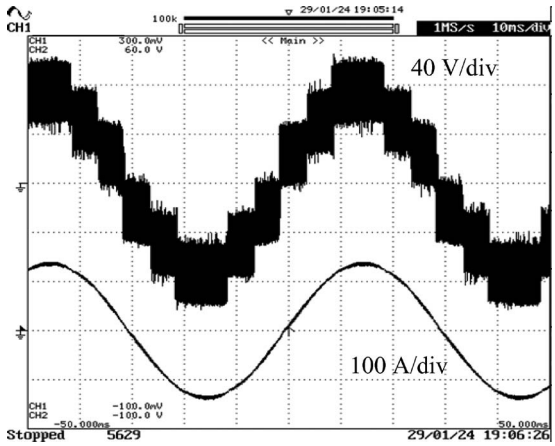


Fig. 13. Phase voltage (over nine levels) and current waveforms with $m = 0.8$.

lying in region ② which requires two BSOs. Both numerical simulations and experimental tests confirm the validity of the multilevel inverter topology as well as the effectiveness of the proposed modulation strategy.

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